The following listing will replace all prior listing of claims in the application.

Listing of Claims:

1. (Previously presented) A method of fabricating a die containing an integrated circuit comprising active components and passive components, the method comprising:

producing a first substrate including at least one active component and producing a second substrate including critical passive components;

bonding the first and second substrates, wherein the bonding comprises performing a layer transfer; and

after bonding of the first and second substrates, producing at least one interconnection line between the components of said first and second substrates, said interconnection line passing through the second substrate.

2. (Previously presented) A method according to claim 1, wherein said at least one active component comprises transistors.

3. (Previously presented) A method according to claim 1, wherein said critical passive components comprise at least one capacitor and at least one microelectromechanical system (MEMS).

4. (Previously presented) A method according to claim 1 wherein said critical passive components comprise at least one capacitor or at least one microelectromechanical system (MEMS).

5. (Previously presented) A method according to claim 3, wherein a dielectric material of said at least one capacitor comprises a perovskite.

6. (Previously presented) A method according to claim 1, wherein producing said second substrate comprises producing an electrically conductive material.

7. (Previously presented) A method according to claim 1, wherein producing said second substrate comprises producing a dielectric material.

8. (Previously presented) A method according to claim 7, wherein producing said second substrate comprises producing perovskite.

9. (Previously presented) A method according to claim 1 further comprising producing dielectric insulation trenches in said second substrate during the production of said second substrate.

10. (Previously presented) A method according to claim 1 further comprising producing at least one non-critical passive component during the production of said second substrate.

11. (Previously presented) A method according to claim 10, wherein producing the non-critical passive component comprises producing a capacitor in trenches.

12. (Previously presented) A method according to claim 9 further comprising producing at least one inductor in the vicinity of a face of the second substrate opposite a bonding face after said bonding of the two substrates.

13. (Previously presented) A method according to claim 12 further comprising producing said at least one inductor on said dielectric insulation trenches.

14. (Cancelled)

15. (Previously presented) A die fabricated by a method according to claim 1.

16. (Previously presented) A die containing an integrated circuit comprising active components and passive components and including a single stack of layers, wherein said die comprises an interface between two of said layers such that a first portion of the die situated on one side of said interface includes at least one active component of said active components and a second portion of said die includes critical passive components of said passive components, the die comprising at least one interconnection line between the components of said first and second portions, said interconnection line passing through the second portion.

17. (Previously presented) A die according to claim 16 wherein said critical passive components comprise at least one capacitor and at least one MEMS enclosed in a cavity situated inside said die.

18. (Cancelled)

19. (Previously presented) A die according to claim 17, wherein the at least one capacitor comprises a dielectric material comprising perovskite.

20. (Previously presented) A die according to claim 16, wherein said die further comprises dielectric insulation trenches.

21. (Previously presented) A die according to claim 16, wherein said integrated circuit further comprises at least one non-critical passive component.

22. (Previously presented) A die according to claim 21 wherein said non-critical passive component comprises a capacitor in trenches.

23. (Previously presented) A die according to claim 16, wherein said active components are disposed in the vicinity of a first face of the die and wherein said integrated circuit further comprises at least one inductor situated in a vicinity of said face of the die opposite said first face.

24. (Previously presented) A die according to claim 23, wherein said at least one inductor is situated on inductive insulation trenches.

25. (Previously presented) A die according to any one of claim 16, wherein said active components are disposed in a vicinity of a first face of said die and said die further comprises at least one interconnection line that emerges in the vicinity of said face of said die opposite said first face.

26. (Previously presented) A die according to any one of claim 21 wherein said active components are disposed in a vicinity of a first face of said die and said die

further comprises at least one interconnection line that emerges in the vicinity of said face of said die opposite said first face.

27. (Previously presented) A method according to claim 13, wherein said at least one inductor and at least one of said interconnection lines are produced during a same process step.